REMARKS/ARGUMENTS

Claims 1-6 are pending in the application. By this amendment, claims 1 and 3 are being amended to improve their form. No new matter is involved.

In paragraph 1 on page 2 of the Office Action, claims 1 and 3 are objected to because of certain informalities which are set forth therein. Claims 1 and 3 are being amended herein by substantially rewriting the portions thereof containing the objectionable matter so that such informalities should no longer exist.

In paragraph 3 on page 2 of the Office Action, claims 1 and 2 are rejected under 35 U.S.C.§ 102(b) as being anticipated by U.S. Patent 5,220,185 of Wada. In paragraph 8 at the bottom of page 3 of the Office Action, claim 3 is rejected under 35 U.S.C.§ 103(a) as being unpatentable over Wada '185 and further in view of PG Pub 2002/0039144 A1 of Yamada. In paragraph 13 at the bottom of page 4 of the Office Action, claims 4 and 6 are rejected under 35 U.S.C.§ 103(a) as being unpatentable over Wada '185 in view of U.S. Patent 5,898,195 of Harada. In paragraph 19 on page 6 of the Office Action, claim 5 is rejected under 35 U.S.C.§ 103(a) as being unpatentable over Wada '185 in view of Harada '195 and further in view of the Yamada publication and still further in view of U.S. Patent 6,018,169 of Tohyama. These rejections are respectfully traversed.

In rejecting claims 1 and 2 as anticipated by Wada '185, the Office Action maintains that all of the structures set forth in such claims are disclosed in the reference. However, "the semiconductor region in the output section" and the "semiconductor region in the horizontal shift register (region 16 in FIG. 1)" in Wada are regions having the same conductive type (N) as that of a semiconductor substrate (11). Thus, Wada fails to disclose the structure of amended claim 1.

In rejecting claims 4-6 on combinations of references which include Harada '195, it should be noted that Harada merely discloses a structure in an overflow drain in a solid image capturing element, and fails to disclose the concentration of dopants in the region of formation of the output section and horizontal shift register in the solid image capturing element.

Claim 1 defines a solid image capturing element comprised of a plurality of vertical shift registers, a horizontal shift register and an output section. As amended herein, claim 1 is further defined in terms of "over one major surface of a semiconductor substrate of one conductive type, a first semiconductor region of an opposite conductive type and a second semiconductor region of the opposite conductive type and having a higher dopant concentration than that of the first semiconductor region are formed." The horizontal shift register is defined as being "formed in the first semiconductor region." The output section is defined as being "formed in the semiconductor region". Therefore, claim 1 is submitted to clearly distinguish patentably over the cited references.

Claims 2 and 3 depend from and contain all of the limitations of claim 1, so that such claims are also submitted to clearly distinguish patentably over the prior art. In the case of claim 3, such claim is being amended herein to recite "over the one major surface of the semiconductor substrate, a third semiconductor region of the opposite conductivity type and having a lower dopant concentration than that of the first semiconductor region is formed, and the plurality of light receiving pixels and the plurality of vertical shift registers are formed in the third semiconductor region".

Claim 4 defines a method for manufacturing a solid image capturing element which includes a first step of forming over one major surface of a conductive

semiconductor substrate a first reverse conductive semiconductor region having a first dopant concentration, a second step of forming over the one major surface of the conductive semiconductor substrate a second reverse conductive semiconductor region having a second dopant concentration which is higher than the first dopant concentration, and a third step of forming the horizontal shift register on the first reverse conductive semiconductor region and the ouput section on the second reverse conductive semiconductor region. Therefore, claim 4 is submitted to clearly distinguish patentably over the cited references.

Claims 5 and 6 depend from and contain all of the limitations of claim 4, so that such claims are also submitted to clearly distinguish patentably over the prior art.

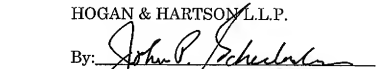
In conclusion, claims 1-6 are submitted to clearly distinguish patentably over the prior art for the reason discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4600 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: December 26, 2007

By: 
John P. Scherlacher
Registration No. 23,009
Attorney for Applicant(s)

1999 Avenue of the Stars, Suite 1400
Los Angeles, California 90067
Phone: 310-785-4600
Fax: 310-785-4601